EXHIBIT B

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May 02, 2022

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APPLICATION NUMBER: *13/288,850*
FILING DATE: *November 03, 2011*
PATENT NUMBER: *8787060*
ISSUE DATE: *July 22, 2014*

UNITED STATES PATENT AND TRADEMARK OFFICE · DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,850	11/03/2011	Hyun Lee	NETL.071A	2466

79141 7590 06/06/2013

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
06/06/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

Office Action Summary	Application No. 13/288,850	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-34* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-34* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Interim copies:

a)☐ All b)☐ Some c)☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-28, drawn to a memory package and a method for optimizing load in a memory package, classified in class 365, subclass 63.

   II. Claims 29-34, drawn to a memory module comprising a register device and a plurality of DRAM packages each comprising a plurality of DDR DRAM dies, classified in class 365, subclass 365/233.13.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the memory module does not require die interconnects having specific functions as recited in claims 1-28. The subcombination has separate utility such as using die interconnects to transmit data to the plurality of array dies.

The examiner has required restriction between combination and subcombination inventions. Where applicant elects a subcombination, and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all

the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply:

Different search;

Different classification; and

Recognized divergent subject matter.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement

will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Huan Hoang/
Primary Examiner, Art Unit 2827

PATENT Customer No. 79141

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hyun Lee
App. No.	:	13/288,850
Filed	:	November 3, 2011
For	:	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS
Examiner	:	ZARABIAN, AMIR
Art Unit	:	2827
Conf. No.	:	2466
Docket No.	:	NETL.071A

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

August 6, 2013

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Restriction Requirement dated June 6, 2013 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 11 of this paper.

IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (**Currently Amended**) A memory package, comprising:

a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;

a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with ~~at least one data port of a first array die of the plurality~~the first group of array dies ~~and at least one data port of a second array die of the plurality of array dies~~ and not in electrical communication with the ~~data ports of at least a third~~second group of at least one array die ~~of the plurality of array dies~~, the second die interconnect in electrical communication with ~~at least one data port of the third~~the second group of at least one array die and not in electrical communication with ~~the data ports of~~ the first group of array dies ~~and the data ports of the second array die~~; and

a control die comprising at least a first data conduit ~~configured to transmit a data signal to~~between the first die interconnect and a first terminal of the plurality of input/output terminals~~and to not transmit the data signal to the second die interconnect~~, and at least a second data conduit ~~configured to transmit the data signal to~~between the second die interconnect and the first terminal ~~and to not transmit the data signal to the first die interconnect~~, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

2. (**Currently Amended**) The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits ~~the first data conduit and the second data conduit are configured to receive the data signal from a common source as one another~~.

3. (**Currently Amended**) The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals ~~a first load on the first data conduit comprises a load of the first die interconnect, a load of the first array die, and a load of the~~

~~second array die, and wherein a second load on the second data conduit comprises a load of the second die interconnect and a load of the third array die~~.

4. (**Currently Amended**) The memory package of claim 3, wherein the control signals include command/address signals and wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies ~~a difference between the first load and the second load is less than a load that would be on the first data conduit upon the first die interconnect being placed in electrical communication with at least one data port of each of the array dies of the plurality of array dies~~.

5. (**Currently Amended**) The memory package of claim 3, wherein:

the first data conduit has a first load that dis less than a load that would be on the first data conduit upon the first die interconnect being placed in electrical communication with at least one data port of each of the array dies of the plurality of array dies; and

the second data conduit has a second load is less than a load that would be on the second data conduit upon the second die interconnect being placed in electrical communication with at least one data port of each of the array dies of the plurality of array dies.

6. (**Currently Amended**) The memory package of claim 1, wherein the first die interconnect comprises a first ~~conducting rod~~through-silicon via and wherein the second die interconnect comprises a second ~~conducting rod~~through-silicon via.

7. (**Currently Amended**) The memory package of claim 1, wherein the control die further comprises chip-select conduits, ~~one of the first die interconnect and the second die interconnect is in electrical communication with at least one data port of a fourth array die of the plurality of array dies and the other one of the first die interconnect and the second die interconnect is not in electrical communication with the data ports of the fourth array die~~ the memory package further comprising:

third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.

8. (**Currently Amended**) The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die

interconnect and a load of the second die interconnect so as to reduce a different between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die ~~is configured to transmit signals to the first array die and the second array die, and to receive signals from the first array die and the second array die, and the second die interconnect is configured to transmit signals to the third array die and to receive signals from the third array die~~.

9. (**Currently Amended**) The memory package of claim 1, further comprising at least a third die interconnect and a fourth die interconnect, the third die interconnect in electrical communication with ~~at least one data port of the first array die and at least one data port of the second array die~~ the first group of array dies and not in electrical communication with the ~~data ports~~ second group of at least ~~the third~~ one array die, the fourth die interconnect in electrical communication with the second group of at least one ~~data port of the third~~ array die and not in electrical communication with the ~~data ports of the first array die and the data ports of the second array die~~first group of array dies.

10. (**Currently Amended**) The memory package of claim 9, wherein the first die interconnect is configured to transmit signals to the first ~~array die and the second array die~~ group of array dies, the second die interconnect is configured to transmit signals to the ~~third~~ second group of at least one array die, the third die interconnect is configured to receive signals from the first ~~array die and the second array die~~ group of array dies, and the fourth die interconnect is configured to receive signals from the ~~third~~ second group of at least one array die.

11. (**Currently Amended**) A memory package, comprising:

a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;

a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die ~~having ports~~;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with ~~at least one port of a first array die of the plurality of~~ the first group of array dies ~~and at least one port of a second array die of the plurality of array dies~~ and not in electrical communication with the ~~ports of at least a third~~ second group of at

least one array die ~~of the plurality of array dies~~, the second die interconnect in electrical communication with ~~at least one port of the third array die~~ the second group of at least one array die and not in electrical communication with the ~~ports of the first array die and the ports of the second array die~~ first group of array dies; and

a control die comprising at least a first data conduit between ~~configured to transmit a signal to~~ the first die interconnect and a first terminal of the plurality of input/output terminals~~to not transmit the signal to the second die interconnect, and~~ , at least a second data conduit ~~configured to transmit the signal to~~ between the second die interconnect and the first terminal ~~to not transmit the signal to the first die interconnect~~, and chip select conduits for providing chip select signals to respective array dies;

~~wherein a first load on the first conduit comprises a load of the first die interconnect, a load of the first array die, and a load of the second array die, and~~

wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals ~~a second load on the second conduit comprises a load of the second die interconnect and a load of the third array die~~.

12. (**Currently Amended**) The memory package of claim 11, wherein the chip select conduits pass through the control die ~~a difference between the first load and the second load is less than a load that would be on the first conduit upon the first die interconnect being placed in electrical communication with at least one port of each of the array dies of the plurality of array dies~~.

13. (**Currently Amended**) The memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies.~~:~~

~~the first load is less than a load that would be on the first conduit upon the first die interconnect being placed in electrical communication with at least one port of each of the array dies of the plurality of array dies; and~~

~~the second load is less than a load that would be on the second conduit upon the second die interconnect being placed in electrical communication with at least one port of each of the array dies of the plurality of array dies~~.

14. (**Currently Amended**) The memory package of claim 11, wherein the first die interconnect comprises ~~a first conducting rod~~ one or more through silicon vias and wherein

the second die interconnect comprises one or more through silicon vias ~~a second conducting rod~~.

15. (**Currently Amended**) The memory package of claim 11, wherein: the first data conduit comprises at least a first driver, and the second data conduit comprises at least a second driver.

16. (**Currently Amended**) The memory package of claim 11~~15~~, wherein the ~~first driver and the second driver are configured to receive the signal from a common source as one another~~control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals.

17. (**Currently Amended**) The memory package of claim 11~~16~~, wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to control signals received via second terminals of the plurality of terminals ~~signal comprises a data signal~~.

18. (**Currently Amended**) The memory package of claim 16, wherein the control signals comprise ~~signal comprises~~ at least one of the following: a command signal, an address signal, and a data path control signal.

19. (**Currently Amended**) The memory package of claim 11, wherein the control die is configured to generate data path control signals from control signals received via second terminals of the plurality of terminals, and wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals ~~16, further comprising a third driver and a fourth driver, wherein the third driver is configured to drive a first signal received from the first die interconnect, and wherein the fourth driver is configured to drive a second signal received from the second die interconnect~~.

20. (**Currently Amended**) A method for optimizing load in a memory package comprising a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die, at least a first die interconnect and a second die interconnect, ~~and~~ a control die, and a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices ~~comprising at least a first driver and a second driver, the first driver configured to~~

~~drive a signal along the first die interconnect, and the second driver configured to drive the signal along the second die interconnect~~, the method comprising:

receiving a data signal at a first terminal of the plurality of input/output terminals;

receiving control signals at second terminals of the plurality of input/output terminals;

providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and

selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.

~~selecting a first subset of array dies of the plurality of array dies and a second subset of array dies of the plurality of array dies, wherein the first subset of array dies and the second subset of array dies are exclusive of one another and are selected to balance a load on the first driver and on the second driver based at least in part on array die loads of array dies of the plurality of array dies and at least in part on die interconnect segment loads of segments of at least the first die interconnect and the second die interconnect;~~

~~forming electrical connections between the first die interconnect and the first subset of array dies; and forming electrical connections between the second die interconnect and the second subset of array dies.~~

21. (**Currently Amended**) The method of claim 20, further comprising:

selecting a first driver size for the first driver based, at least in part, on ~~the~~ a load on the first driver; and

selecting a second driver size for the second driver based, at least in part, on ~~the~~ a load on the second driver.

22. (**Currently Amended**) The method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive ~~the~~ a signal along a die interconnect in electrical communication with each of the plurality of array dies ~~with a less than predetermined~~without significant signal degradation.

23. (**Currently Amended**) The method of claim 20, further comprising generating the chip select signals from at least some of the control signals ~~wherein each array die of the plurality of array dies comprises a substantially equal array die load~~.

24. (**Currently Amended**) The method of claim 20, wherein the control signals include the chip-select signals ~~each segment of the first die interconnect and the second die interconnect comprises a substantially equal die interconnect segment load~~.

25. (**Currently Amended**) The method of claim 20, wherein the ~~segments of the die interconnect comprise one or more portions of a die interconnect between two adjacent array dies~~first and second die interconnects each comprises at least one through silicon vias.

26. (**Currently Amended**) The method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die ~~the segments of the die interconnect comprise one or more portions of a die interconnect between the control die and an adjacent array die~~.

27. (**Currently Amended**) The method of claim 20, further comprising generating data path control signals from at least some of the control signals, the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal~~wherein the first subset of array dies comprises at least two array dies~~.

28. (**Currently Amended**) The method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals ~~balancing the load on the first driver and the load on the second driver comprises minimizing a load difference between the first driver and the second driver~~.

29. (**Currently Amended**) A memory module operable via a memory control hub, comprising:

a register device configured to receive command/address signals from the ~~a~~ memory control hub and to generate ~~data path~~ control signals; and

a plurality of DRAM packages, each DRAM package comprising:

a plurality of data terminals via which the DRAM package communicate data with the memory control hub, and a plurality of control terminals to receive the control signals;

a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

~~a control die comprising a plurality of command/address buffers and a data path control circuit configured to control command/address time slots and data bus time slots, the control die configured to receive data signals from the memory control hub, the data path control signals from the register device, and command/address signals from the register device; and~~

~~a plurality of DDR DRAM dies operatively coupled to the control die to receive the data signals from the control die, wherein the memory module is selectively configurable into at least~~

~~two operational modes comprising:~~

~~a first operational mode in which the register device generates the data path control signals, and the control die uses the data path control signals to operate the data path control circuit; and~~

~~a second operational mode in which the control die operates the data path control circuit to provide the command/address signals to the plurality of DDR DRAM dies without decoding the command/address signals~~.

30. (**Currently Amended**) The memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals.

31. (**Currently Amended**) The memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit ~~memory module does not perform rank multiplication while operating in the second operational mode~~.

32. (**Currently Amended**) The memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals.

33. (**Currently Amended**) The memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals ~~at least one of the plurality of DRAM packages comprises the memory package of claim 1~~.

34. (**Currently Amended**) The memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit ~~at least one of the plurality of DRAM packages comprises the memory package of claim 11~~.

REMARKS

This amendment responds to the Restriction Requirement mailed June 6, 2013. Applicant would like to elect without traverse the invention in Claims 1-28 as amended for examination.

I. McKesson Statement

The pending application is related to commonly owned U.S. Patent Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097, 7,839,645, 7,864,627, 7,881,150, 8,001,434, 8.033.836, 8,154,901, 8,417,870, 8,489,837, and 8516185, and U.S. Patent Application 12/422,912. The Examiner is encouraged to review the art made of record, Office Action(s) and the Notice of Allowance in the above-mentioned related application, all of which are available on PAIR.

II. Amendments to the Claims

Claims 1-28 have been amended to better define the inventions which the Applicant intends to claim in the present application. Claims 29-34 have been amended to include the particulars of claims 11-19 so that they relate to the same subject matter as claims 11-19. Thus, claims 29-34 should no longer be subject to restriction requirement. No new matter is added.

The Examiner is invited to call the undersigned attorney at (650) 273-6008, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: August 6, 2013

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

UNITED STATES PATENT AND TRADEMARK OFFICE

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79141 7590 10/11/2013

The Law Office of Jamie Zheng, Ph.D Esq.
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jz@jzpatent.com

Office Action Summary	Application No. 13/288,850	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-34* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-7,9-21 and 23-34* is/are rejected.

8)☒ Claim(s) *8 and 22* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11/03/11* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/23/12, 04/25/13*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-28 in the reply filed on 08/06/13 is acknowledged.

Claims 29-34 have been amended to include the particulars of claims 11-19 so that they relate to the same subject matter as claims 11-19. Accordingly, the restriction requirement is withdrawn.

Information Disclosure Statement

2. The document "A Quantitative Analysis of Performance Benefits of 3D Die Stacking on Mobile and Embedded SoC" in the information disclosure statement filed 05/23/2012 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because a date has not been provided. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based

on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

3. The cite No.36 in the IDS filed on 05/23/12 has not been considered. It should be 2008/0025137 and has been cited in Form PPTO-892.

Claim Objections

4. Claim 5 is objected to because of the following informalities:

The word "dis" in claim 5, line 2 should be "is" and the term "different" in claim 8, line 4 should be "difference". Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 5 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

The recitation of "the first data conduit has a first load that hat is less than a load that would be on the first data conduit upon the first die interconnect being placed in electrical communication with at least one data port of each of the array dies of the

plurality of array dies; and the second data conduit has a second load is less than a load that would be on the second data conduit upon the second die interconnect being placed in electrical communication with at least one data port of each of the array dies of the plurality of array dies." is confusing since the first die interconnect/the second die interconnect is only in electrical communication with the first group of array dies/the second group of at least one die; therefore, the first die interconnect/the second die interconnect cannot be in electrical communication with each of the array dies (at least one array die of the second group is not in electrical communication with the first die interconnect and the array dies of the first group are not in electrical communication with the with the second die interconnect).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33 and 34 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Rajan et al. (US 2008/0025137).

Regarding claim 1: Rajan (Fig. 2B) shows a memory package, comprising:

a plurality of input/output terminals (address, Control, Clock and Data) via which the memory package communicate data and control/address signals with one or more external devices;

a plurality of stacked array dies (paragraph [0043], lines 1-3) including a first group of array dies (206A and 206C) and a second group (206B and 206D) of at least one array die, each array die having data ports;

at least a first die interconnect (Data connected to 206A and 206C) and a second die interconnect (Data connected to 206B and 206D), the first die interconnect in electrical communication with first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die (BUFFER CHIP) comprising at least a first data conduit between the first die interconnect and a first terminal (Data) of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit (paragraph [0044], lines 5-7) to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals (Address, Clock and Control).

Regarding claims 2-4: Rajan discloses the memory package of claim 1, wherein the control signals include data path control signals (Control, Address and Clock must be used to address the DRAM circuits and control the data between Data terminal to DRAM circuits) for controlling the first and second data conduits.

Regarding claims 7, 11, 12 and 16-19: Rajan discloses the memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising:

Regarding claims 9 and 10, the third die interconnect and the fourth die interconnect are considered the first die interconnect and the second die interconnect, respectively.

third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies (paragraph [0057], lines 7-13).

Regarding claims 13 and 15: It is inherent that there are drivers to drive data from BUFFER CHIP to DRAM circuits.

Regarding claim 20: Rajan (Fig. 2B) discloses a method for optimizing load in a memory package comprising a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die, at least a first die interconnect and a second die interconnect, a control die, and a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices, the method comprising:

receiving a data signal at a first terminal (Data) of the plurality of input/output terminals;

receiving control signals (Address, Control and Clock) at second terminals of the plurality of input/output terminals;

providing chip select signals (paragraph [0057], lines 7-13) to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and

selecting one of a first driver and a second driver (it is inherent that there are drivers to drive data from BUFFER CHIP to DRAM circuits) in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.

are exclusive of one another and are selected to balance a load on the first driver and on the second driver based at least in part on array die loads of array dies of the plurality of array dies and at least in part on die interconnect segment loads of segments of at least the first die interconnect and the second die interconnect; forming electrical connections between the first die interconnect and the first subset of array dies; and forming electrical connections between the second die interconnect and the second subset of array dies

Regarding claim 21: It is inherent to select a drive size for a drive based on a load on the driver.

Regarding claims 23, 24, 27 and 28: Rajan discloses the method of claim 20, further comprising generating the chip select signals from at least some of the control

signals (the chip select signals are used to select the DRAM circuits; therefore, the chip select signals are generated from address bits, paragraph [0057], lines 7-13).

Regarding claims 29, 31, 33 and 34: Rjan discloses a memory module operable via a memory control hub, comprising:

a register device (paragraph [0076], lines 6-8) configured to receive command/address signals from the memory control hub and to generate control signals; and

a plurality of DRAM packages, each DRAM package comprising: a plurality of data terminals via which the DRAM package communicate data with the memory control hub, and a plurality of control terminals to receive the control signals; a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals (paragraph [0057], lines 7-13).

Claim Rejections - 35 USC § 103

9. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6, 14, 25 and 26 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rajan in view of Kirby et al. (US 2011/0193226, hereinafter “Kirby”).

The only difference between claims 6. 25 and 26 and Rajan is that the first and second die interconnects each comprising at least one through silicon vias. However, Kirby discloses the use of a through-silicon via for a conductive component for interconnecting with an external component (paragraph [0036], lines 7-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a through-silicon via as a die interconnect for interconnecting the memory package with an external component.

11. Claims 30 and 32 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rajan in view of Gervasi (US 2006/0259678).

Claims 30 and 32 differ from Rajan in reciting that the register device or the control die is configured to perform rank multiplication by generating the ship select from the control signals. However, Gervasi discloses a register distributing the address and controls to the RAM chips to perform rank multiplication (paragraph [0044], lines 1-5.) It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a register device to perform rank multiplication from the control signals

Allowable Subject Matter

12. Claims 8 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

.The following is a statement of reasons for the indication of allowable subject matter:

.Regarding claim 8: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of “wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a different between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die

interconnect and a load of the second group of at least one array die" in combination with the other limitations thereof as is recited in the claim.

Regarding claim 22: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation." in combination with the other limitations thereof as is recited in the claim.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Huan Hoang/
Primary Examiner, Art Unit 2827

PATENT Customer No. 79141

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Hyun Lee
App. No.	:	13/288,850
Filed	:	November 3, 2011
For	:	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS
Examiner	:	ZARABIAN, AMIR
Art Unit	:	2827
Conf. No.	:	2466
Docket No.	:	NETL.071A

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

January 13, 2014

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Non-Final Office Action dated October 11, 2013 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 9 of this paper.

IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (**Previously Presented**) A memory package, comprising:

a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;

a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

2. (**Previously Presented**) The memory package of claim 1, wherein the control signals include data path control signals for controlling the first and second data conduits.

3. (**Previously Presented**) The memory package of claim 1, wherein the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals.

4. (**Previously Presented**) The memory package of claim 3, wherein the control signals include command/address signals and wherein the control die is configured to provide the command/address signals to the plurality of stacked array dies.

5. (**Cancelled**)

6. (**Previously Presented**) The memory package of claim 1, wherein the first die interconnect comprises a first through-silicon via and wherein the second die interconnect comprises a second through-silicon via.

7. (**Previously Presented**) The memory package of claim 1, wherein the control die further comprises chip-select conduits, the memory package further comprising:

third die interconnects coupled between respective chip-select conduits and respective ones of the plurality of stacked array dies.

8. (**Currently Amended**) The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference ~~different~~ between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.

9. (**Cancelled**)

10. (**Cancelled**)

11. (**Previously Presented**) A memory package, comprising:

a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;

a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, at least a second data conduit between the second die interconnect and the first terminal, and chip select conduits for providing chip select signals to respective array dies;

wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

12. (**Previously Presented**) The memory package of claim 11, wherein the chip select conduits pass through the control die.

13. (**Previously Presented**) The memory package of claim 11, wherein the chip select conduits include drivers to drive the chip select signals to the respective array dies.

14. (**Previously Presented**) The memory package of claim 11, wherein the first die interconnect comprises one or more through silicon vias and wherein the second die interconnect comprises one or more through silicon vias.

15. (**Currently Amended**) The memory package of claim 11, wherein: the first data conduit comprises at least a first driver having a first driver size, and the second data conduit comprises at least a second driver having a second driver size, and wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

16. (**Currently Amended**) The memory package of claim 11, wherein the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using an address signal in the control/address signals.

17. (**Currently Amended**) The memory package of claim 11, wherein the control circuit controls the respective states of the first data conduit and the second data conduit in response to at least some of the control/address signals received via second terminals of the plurality of terminals.

18. (**Currently Amended**) The memory package of claim 16, wherein the control/address signals comprise ~~at least one of the following:~~ ~~a~~ at least one command signal, ~~an~~ at least one address signal, and ~~a~~ at least one data path control signal.

19. (**Currently Amended**) The memory package of claim 11, wherein the control die is configured to generate data path control signals from the control/address signals received via

second terminals of the plurality of terminals, and wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals.

20. (**Previously Presented**) A method for optimizing load in a memory package comprising a plurality of array dies arranged in a stack and including a first group of array dies and a second group of at least one array die, at least a first die interconnect and a second die interconnect, a control die, and a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices, the method comprising:

receiving a data signal at a first terminal of the plurality of input/output terminals;

receiving control signals at second terminals of the plurality of input/output terminals;

providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and

selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.

21. (**Previously Presented**) The method of claim 20, further comprising:

selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and

selecting a second driver size for the second driver based, at least in part, on a load on the second driver.

22. (**Previously Presented**) The method of claim 21, wherein the first driver size and the second driver size are both less than a driver size sufficient to drive a signal along a die interconnect in electrical communication with each of the plurality of array dies without significant signal degradation.

23. (**Previously Presented**) The method of claim 20, further comprising generating the chip select signals from at least some of the control signals.

24. (**Previously Presented**) The method of claim 20, wherein the control signals include the chip-select signals.

25. (**Previously Presented**) The method of claim 20, wherein the first and second die interconnects each comprises at least one through silicon vias.

26. (**Previously Presented**) The method of claim 20, wherein the chip select signals pass through through-silicon-vias in the control die.

27. (**Previously Presented**) The method of claim 20, further comprising generating data path control signals from at least some of the control signals, the data path control signals being used to select the one of the first driver and the second driver in the control die to drive the data signal.

28. (**Previously Presented**) The method of claim 20, wherein the one of the first driver and the second driver is selected using at least some of the control signals.

29. (**Previously Presented**) A memory module operable via a memory control hub, comprising:

a register device configured to receive command/address signals from the memory control hub and to generate control signals; and

a plurality of DRAM packages, each DRAM package comprising:

a plurality of data terminals via which the DRAM package communicate data with the memory control hub, and a plurality of control terminals to receive the control signals;

a plurality of array dies arranged in a stack, including a first group of array dies and a second group of at least one array die;

at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising at least a first data conduit between the first die interconnect and a first data terminal of the plurality of data terminals, at least a second data conduit between the second die interconnect and the first data terminal, and chip select conduits for providing chip select signals to respective array dies, the chip select signals being related to at least some of the control signals;

wherein the control die further comprises a control circuit to control respective states of the first data conduit and the second data conduit to drive a data signal to an array die selected by at least one of the chip-select signals.

30. (**Previously Presented**) The memory module of claim 29, wherein the register device is further configured to perform rank multiplication by generating the chip select signals, and wherein the control signals include the chip select signals.

31. (**Previously Presented**) The memory module of claim 29, wherein the control signals include data path control signals generated by the register device, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

32. (**Currently Amended**) The memory module of claim 29, wherein the control die is further configured to perform rank multiplication by generating the chip select signals from at least some of the control signals that include at least one address signal.

33. (**Previously Presented**) The memory module of claim 29, wherein the control signals include command/address signals, and the control die is configured to hold the command/address signals to control timing of the command/address signals.

34. (**Previously Presented**) The memory module of claim 29, wherein the control die is configured to generate data path control signals from at least some of the control signals, the data path control signals being used to control the respective states of the first data conduit and the second data conduit.

35. (**New**) The memory package of claim 1, wherein the respective states of the first data conduit and the second data conduit are controlled by one or more data path control signals, wherein the control die is configurable to operate in any one of a first mode and a second mode, and wherein:

in the first mode, the control die receives the data path control signals from the one or more external devices; and

in the second mode, the control die generates the data path control signals from at least some of the control/address signals received from the one or more external devices.

36. (**New**) The memory package of claim 1, wherein the control die further comprises command/address conduits configured to provide corresponding command/address signals to the array dies, the command/address signals including at least one memory cell address.

37. (**New**) The memory package of claim 1, wherein the control die further comprises one or more additional conduits configured to provide one or more of a supply voltage signal and a ground signal to the array dies.

REMARKS

This amendment responds to the Non-Final Office Action dated October 11, 2013. In the Office Action, the Examiner:

- withdrew the restriction requirement of claims 29-34;
- noted two issues with the Information Disclosure Statement submitted on 5/23/2012;
- objected to informalities in claim 5 and claim 8;
- rejected claim 5 under 35 U.S.C. 112(b) or 35 U.S.C.112 (pre-AIA), second paragraph as being indefinite;
- rejected claims 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33, and 34 under pre-AIA 35 U.S.C. 102(b) as being anticipated by Rajan et al. (US 2008/0025137);
- rejected claims 6, 14, 25, and 26 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rajan in view of Kirby et al. (US 2011/0193226);
- rejected claims 30 and 32 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Rajan in view of Gervasi (US 2006/0259678); and
- objected to claims 8 and 22 as being dependent upon a rejected base claim.

Applicant appreciates the allowance of claims 8 and 22 if rewritten in independent form, but would like to request reconsideration of the rejected claims in light of the amendments and remarks.

I. CLAIM AMENDMENT

Claims 5, 9 and 10 are cancelled. Claims 8, 15-19 and 32 are amended. New claims 35-37 are presented. No new matter is added.

II. INFORMATION DISCLOSURE STATEMENT SUBMITTED ON 5/23/2012

The Examiner noted that the document "A Quantitative Analysis of Performance Benefits of 3D Die Stacking on Mobile and Embedded SoC" in the information statement filed 05/23/2012 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because a date has not been provided. Base on a recent Internet search, this article appears to have been published in 978-3-9810801-7-9/DATE11/©2011 EDAA (http://www.date-

conference.com/proceedings/PAPERS/2011/DATE11/PDFFILES/10.7_4.PDF). So, the year of publication is 2011. The exact date of this publication, however, is unknown to the Applicant.

III. OBJECTION TO INFORMALITIES IN CLAIM 5 AND CLAIM 8

Claim 5 is cancelled. Claim 8 is amended to cure the informalities. Therefore, the objection to claim 5 is moot and the objection to claim 8 should be withdrawn.

IV. REJECTION OF CLAIM 5 UNDER 35 U.S.C. 112(B) OR 35 U.S.C.112 (PRE-AIA), SECOND PARAGRAPH

Claim 5 is cancelled. Therefore, the rejection thereof is moot.

V. REJECTION OF CLAIMS 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33, AND 34 UNDER PRE-AIA 35 U.S.C. 102(B) AS BEING ANTICIPATED BY RAJAN ET AL. (US 2008/0025137)

Claim 1 recites:

> A memory package, comprising:
> a plurality of input/output terminals via which the memory package communicate data and control/address signals with one or more external devices;
> a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;
> at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
> a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

First of all, Rajan does not disclose "a plurality of stacked array dies." Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim 1. In rejecting claim 1, the Examiner states that Rajan (FIG. 2B) shows a memory package as recited in

claim 1. The Examiner further cites Paragraph [0044] as disclosing the control die as recited in claim 1. Paragraph [0044] in Rajan, however, merely states:

> As shown in each of such figures, the buffer chip 202 is placed electrically between an electronic host system 204 and a stack of DRAM circuits 206A-D. In the context of the present description, a stack may refer to any collection of memory circuits. Further, the buffer chip 202 may include any device capable of buffering a stack of circuits (e.g. DRAM circuits 206A-D, etc.). Specifically, the buffer chip 202 may be capable of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system 204. In this way, the stack of DRAM circuits 206A-D may appear as a smaller quantity of larger capacity DRAM circuits to the host system 204.

Thus, the statements in this paragraph [0044] of Rajan says nothing about the existence of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals." According to this paragraph [0044], all that is required of the buffer chip 202 is the capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system, and this requirement does not necessitate the use of a first data conduit and a second data conduit in the buffer chip 202 and "a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."

Furthermore, according to paragraphs [0043] and [0044], this same capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system is required for each of the FIGS. 2A-2E, which show various configurations of a buffered stack of DRAM circuits 206A-D with the buffer chip 202. Since FIG. 2D of Rajan shows a single data bus between the buffer chip and all of the stacked DRAM circuits 206A-D (*Rajan, paragraph [0051]*), this capability of buffering the stack of DRAM circuits 206A-D, which also applies to the configuration in FIG. 2D, can not be said to imply the existence of first and second data conduits in the buffer chip 202 and a control circuit controlling the respective states of the first data conduit and the second data conduit in response to any received control signals, because the first and second data conduits would be coupled to a same data line in the single data bus in FIG. 2D and it would make no sense to try to control respective states or the first data conduit and the second data conduit.

Therefore, Rajan fails to disclose each and every limitation in claim 1, and claim 1 is patentable over Rajan.

Claims 2-4 and 7 depend from claim 1 and include further limitations in addition to the limitations in claim 1. Therefore, claims 2-4 and 7 are patentable for at least the same reasons claim 1 is patentable.

Claims 2-4 and 7 are also patentable for the additional features recited therein. For example, claim 2 includes the further limitations that the control signals received via the one or more second terminals of the plurality of terminals include data path control signals for controlling the first and second data conduits. Rajan does not disclose any data path control signals. In Rajan, besides the data signals, the signals the buffer chip receives are address/control/clock signals (*Rajan, Paragraph [0025]*). These are signals used for memory operations, not for controlling any data conduits in the buffer chip 202.

As a further example, claim 3 recites "the control circuit is configured to generate data path control signals for controlling the first and second data conduits in response to the received control signals." As stated above, Rajan does not disclose any data path control signals. Therefore, Rajan cannot be said to disclose anything about generating the data path control signals in its buffer chip 202.

Claims 9-10 are cancelled. Therefore, the rejections thereof are moot.

The arguments regarding claim 1 applies to claim 11. Therefore, claim 11 is also patentable over Rajan.

Claims 12-13, and claims 15-19 as amended depend from claim 11 and include further limitations in addition to the limitations in claim 11. Therefore, claims 12-13, and claims 15-19 as amended are patentable for at least the same reasons claim 11 is patentable.

Claims 12-13, and claims 15-19 as amended are also patentable for the additional features recited therein. For example, claim 15 is amended to include certain features in claim 22, which are considered allowable.

Claim 16 as amended recites that the control die is configured to generate the chip select signals from control signals received via second terminals of the plurality of terminals, and wherein the chip select signal is generated using at least one address signal in the

control/address signals. Rajan does not teach generating chip select signals in the buffer chip 202, let alone generating chip select signals using a received address signal.

Claim 18 as amended recites that the control/address signals comprise: at least one command signal, at least one address signal, and at least one data path control signal. Again Rajan does not teach data path control signal, nor does Rajan teaches receiving such signals at the buffer chip 202.

Claim 19 as amended recites that the control die is configured to generate data path control signals from the control/address signals received via second terminals of the plurality of terminals, and wherein the control circuit controls the respective states of the first data conduit in response to the data path control signals. Again, Rajan does not teach data path control signals, let alone generating such signals as the buffer chip from received control/address signals.

Claim 20 recites, among other things:

> selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies

Rajan does not teach these limitations. As stated above, Rajan only requires its buffer chip 202 to buffer the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system, and this same requirement is applicable for each of the FIGS. 2A-2E (*Rajan, paragraphs [0043] and[0044]*). Since FIG. 2D shows that all of the DRAM circuits 206A-D are coupled to the buffer chip 202 via a same data bus, this requirement cannot be used to infer that the buffer chip 202 has to select "one of a first driver and a second driver to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals." Therefore, Rajan does not disclose each and every limitations in claim 20, and claim 20 is patentable over Rajan.

Claims 21, 23-24, and 27-28 depend from claim 20 and include further limitations in addition to the limitations in claim 20. Therefore, claims 21, 23-24, and 27-28 are patentable for at least the same reasons claim 20 is patentable.

The arguments regarding claim 1 is applicable to claim 29. Therefore, claim 29 is also patentable over Rajan.

Claims 31 and 33-34 depend from claim 29 and include further limitations in addition to the limitations in claim 29. Therefore, claims 31 and 33-34 are patentable for at least the same reasons claim 20 is patentable.

VI. REJECTION OF CLAIMS 6, 14, 25-26, 30 AND 32 UNDER PRE-AIA 35 U.S.C. 103(A)

Claims 6 and 14 depend from claims 1 and 11, respectively, and include further limitations in addition to the limitations in claims 1 and 11, respectively. Therefore, claims 6 and 14 are patentable for at least the same reasons claims 1 and 11, respectively, are patentable.

Claims 25-26 depend from claim 20 and include further limitations in addition to the limitations in claim 20. Therefore, claims 25-26 are patentable for at least the same reasons claim 20 is patentable.

Claim 30 and claim 32 as amended depend from claim 29 and include further limitations in addition to the limitations in claim 29. Therefore, claim 30 and claim 32 are patentable for at least the same reasons claim 20 is patentable.

VII. NEW CLAIMS 35-37

New claims 35-37 depend from claim 1, and include further limitations in addition to the limitations in claim 1. Therefore, new claims 35-37 are patentable for at least the same reasons claim 1 is patentable.

VIII. NO DISCLAIMERS OR DISAVOWALS

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter

supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

IX. SUMMARY

At least for the foregoing reasons, Applicant submits that claims 1-4, 6-8, and 11-37 are in condition for allowance, and Applicant respectfully requests such action. The Examiner is invited to call the undersigned at (650) 273-6008 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: January 13, 2014

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 03/26/2014

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
HOANG, HUAN	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/26/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,850	11/03/2011	Hyun Lee	NETL.071A	2466

TITLE OF INVENTION: METHOD AND APPARATUS FOR OPTIMIZING DRIVER LOAD IN A MEMORY PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/26/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 03/26/2014
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/288,850	11/03/2011	Hyun Lee	NETL.071A	2466

TITLE OF INVENTION: METHOD AND APPARATUS FOR OPTIMIZING DRIVER LOAD IN A MEMORY PACKAGE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	06/26/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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79141 7590 03/26/2014

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/26/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 151 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 151 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/288,850	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed on 01/14/14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-4,6-8 and 11-37*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   Certified copies:
   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the claims:

Claim 1, line 2, replace "communicate" with –communicates--;

Claim 11, line 2, replace "communicate" with –communicates--;

Claim 20, line 5, replace "communicate" with –communicates--; and

Claim 29, line 6, replace "communicate" with –communicates--.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827